

# 54ACQ/74ACQ244 • 54ACTQ/74ACTQ244

## Quiet Series Octal Buffer/Line Driver with TRI-STATE® Outputs

### General Description

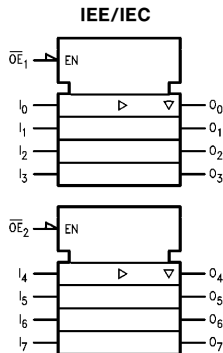
The 'ACQ/'ACTQ244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The ACQ/ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

### Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- TRI-STATE® outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT244
- 4 kV minimum ESD immunity
- Standard Military Drawing (SMD)
  - 'ACTQ244: 5962-8776003
  - 'ACQ244: 5962-92176

54ACQ/74ACQ244 • 54ACTQ/74ACTQ244  
Quiet Series Octal Buffer/Line Driver with TRI-STATE Outputs

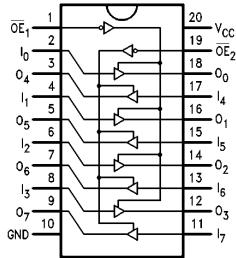
### Logic Symbol



TL/F/10235-1

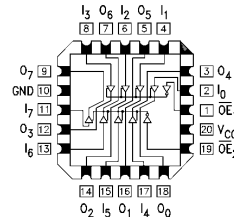
### Connection Diagrams

Pin Assignment for DIP, Flatpak, QSOP and SOIC



TL/F/10235-2

Pin Assignment for LCC



TL/F/10235-3

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$O_0-O_7$	Outputs

### Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	$I_n$	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	$I_n$	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level      X = Immaterial  
L = LOW Voltage Level      Z = High Impedance

TRI-STATE® is a registered trademark of National Semiconductor Corporation. FACT™, FACT Quiet Series™, and GTO™ are trademarks of National Semiconductor Corporation.

## Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 300$ mA
Junction Temperature ( $T_J$ )	
CDIP	175°C
PDIP	140°C

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	2.0V to 6.0V
'ACQ	4.5V to 5.5V
'ACTQ	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
74ACQ/ACTQ	-40°C to +85°C
54ACQ/ACTQ	-55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACQ Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACTQ Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note:** All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to +125°C.

## DC Electrical Characteristics for 'ACQ Family Devices

Symbol	Parameter	$V_{CC}$ (V)	74ACQ			54ACQ			74ACQ			Units	Conditions
			$T_A = +25^\circ\text{C}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				
			Typ	Guaranteed Limits									
$V_{IH}$	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$				
		4.5	2.25	3.15	3.15	3.15							
		5.5	2.75	3.85	3.85	3.85							
$V_{IL}$	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$				
		4.5	2.25	1.35	1.35	1.35							
		5.5	2.75	1.65	1.65	1.65							
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$				
		4.5	4.49	4.4	4.4	4.4							
		5.5	5.49	5.4	5.4	5.4							
		3.0		2.56	2.4	2.46	V	* $V_{IN} = V_{IL}$ or $V_{IH}$ -12 mA $I_{OH} = -24 \text{ mA}$ -24 mA					
		4.5		3.86	3.7	3.76							
		5.5		4.86	4.7	4.76							
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$					
		4.5	0.001	0.1	0.1	0.1							
		5.5	0.001	0.1	0.1	0.1							
		3.0		0.36	0.50	0.44	V	* $V_{IN} = V_{IL}$ or $V_{IH}$ 12 mA $I_{OL} = 24 \text{ mA}$ 24 mA					
		4.5		0.36	0.50	0.44							
		5.5		0.36	0.50	0.44							
$I_{IN}$	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	$V_I = V_{CC}, \text{GND}$ (Note 1)					
$I_{OLD}$	†Minimum Dynamic Output Current	5.5			50	75	mA	$V_{OLD} = 1.65V \text{ Max}$					
$I_{OHD}$		5.5			-50	-75	mA	$V_{OHD} = 3.85V \text{ Min}$					
$I_{CC}$	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND (Note 1)					

\*All outputs loaded thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

## DC Electrical Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74ACQ		54ACQ	74ACQ		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -55°C to +125°C	T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits					
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	5.5		±0.25	±5.0	±2.5		μA	V <sub>I(OE)</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.1	1.5				V	Figures 2-12, 13 (Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-0.6	-1.2				V	Figures 2-12, 13 (Notes 2, 3)
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5				V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5				V	(Notes 2, 4)

**Note 1:** I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

**Note 2:** Plastic DIP package.

**Note 3:** Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

**Note 4:** Max number of Data Inputs (n) switching. (n - 1) Inputs switching 0V to 5V (ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	74ACTQ		54ACTQ	74ACTQ		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -55°C to +125°C	T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits					
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	2.0	2.0	2.0	2.0		
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	0.8	0.8	0.8	0.8		
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	4.4	V	I <sub>O</sub> = -50 μA
		5.5	5.49	5.4	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA -24 mA
		5.5		4.86	4.70	4.76			
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	0.1	V	I <sub>O</sub> = 50 μA
		5.5	0.001	0.1	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA 24 mA
		5.5		0.36	0.50	0.44	0.44		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	5.5		±0.25	±5.0	±2.5		μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND
I <sub>CC</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.6	1.5		mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	† Minimum Dynamic Output Current	5.5			50	75		mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>		5.5			-50	-75		mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 1)
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.1	1.5				V	Figures 2-12, 13 (Notes 2, 3)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-0.6	-1.2				V	Figures 2-12, 13 (Notes 2, 3)

\*All outputs loaded thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

## DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74ACTQ		54ACTQ	74ACTQ	Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -55°C to +125°C	T <sub>A</sub> = -40°C to +85°C		
			Typ	Guaranteed Limits				
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

**Note 1:** I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

**Note 2:** Plastic DIP package.

**Note 3:** Max number of outputs defined as (n). Data Inputs are driven 0V to 3V. One output @ GND.

**Note 4:** Max number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACQ			54ACQ		74ACQ		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Data to Output	3.3	2.0	7.0	9.0	1.0	12.5	2.0	9.5	ns
		5.0	1.5	5.0	6.0	1.0	9.0	1.5	6.5	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	3.3	2.5	8.0	12.0	1.0	12.0	2.5	12.5	ns
		5.0	1.5	6.5	8.0	1.0	10.0	1.5	8.5	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	3.3	1.0	9.0	13.5	1.0	11.5	1.0	14.0	ns
		5.0	1.0	7.5	9.0	1.0	10.0	1.0	9.5	
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns
		5.0		0.5	1.0				1.0	

\*Voltage Range 5.0 is 5.0V ±0.5V.

Voltage Range 3.3 is 3.3V ±0.3V.

\*\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACTQ			54ACTQ		74ACTQ		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Data to Output	5.0	1.5	5.5	6.5	1.5	9.0	1.5	7.0	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	5.0	1.5	7.0	8.5	1.5	10.5	1.5	9.0	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	5.0	1.0	8.0	9.5	1.5	10.5	1.0	10.0	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew** Data to Output	5.0		0.5	1.0				1.0	ns

\*Voltage Range 5.0 is 5.0V ±0.5V.

\*\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = OPEN$
$C_{PD}$	Power Dissipation Capacitance	70	pF	$V_{CC} = 5.0V$

## FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator  
 PC-163A Test Fixture  
 Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set  $V_{CC}$  to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

$V_{OLP}/V_{OLV}$  and  $V_{OHP}/V_{OHV}$ :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure  $V_{OLP}$  and  $V_{OLV}$  on the quiet output during the HL transition. Measure  $V_{OHP}$  and  $V_{OHV}$  on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

$V_{ILD}$  and  $V_{IHD}$ :

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level,  $V_{IL}$ , until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input LOW voltage level at which oscillation occurs is defined as  $V_{ILD}$ .
- Next increase the input HIGH voltage level on the word generator,  $V_{IH}$  until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input HIGH voltage level at which oscillation occurs is defined as  $V_{IHD}$ .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

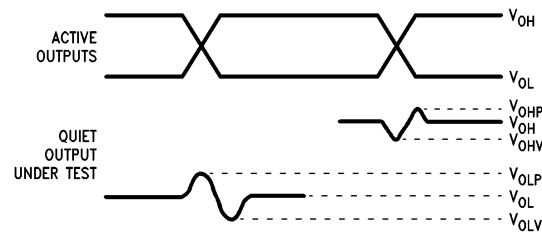


FIGURE 1. Quiet Output Noise Voltage Waveforms

TL/F/10235-4

**Note A.**  $V_{OHV}$  and  $V_{OLP}$  are measured with respect to ground reference.

**Note B.** Input pulses have the following characteristics:  $f = 1$  MHz,  $t_r = 3$  ns,  $t_f = 3$  ns, skew < 150 ps.

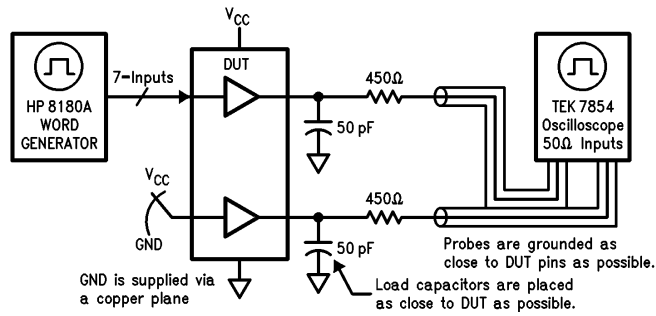
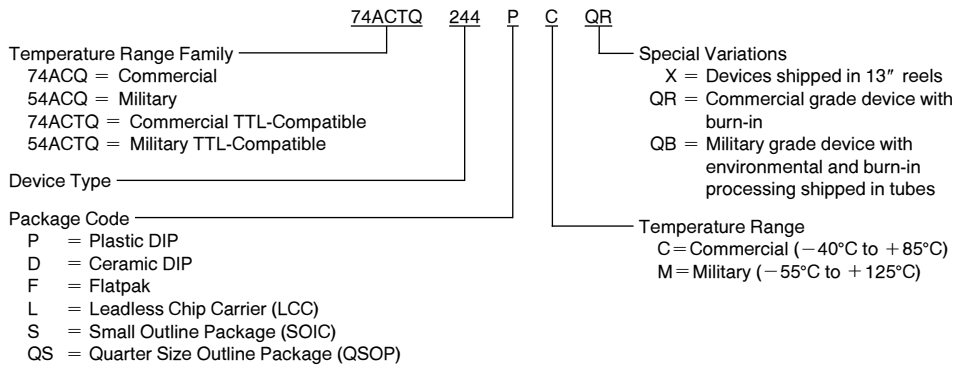


FIGURE 2. Simultaneous Switching Test Circuit

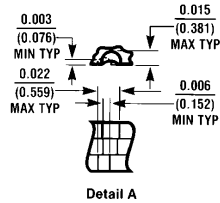
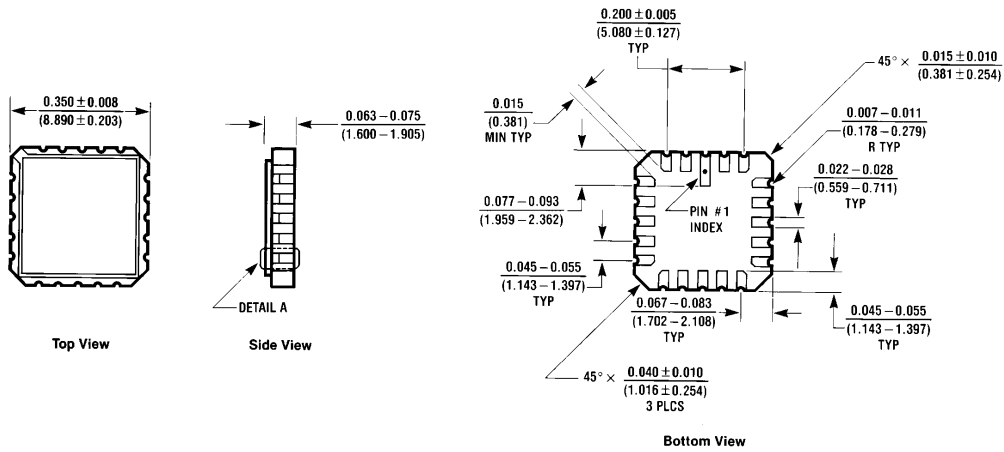
TL/F/10235-5

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

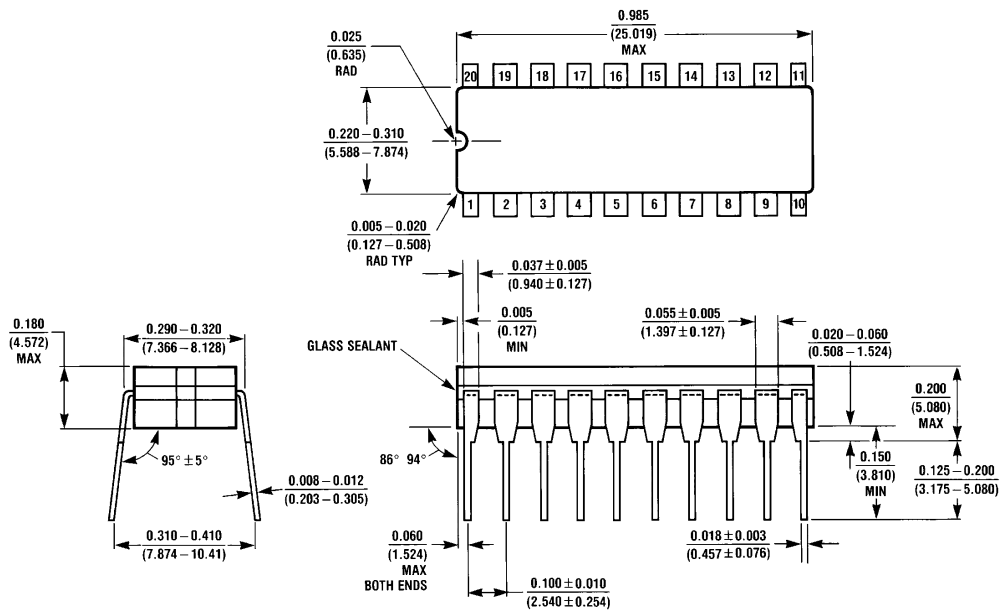


**Physical Dimensions** inches (millimeters)



**20-Terminal Ceramic Leadless Chip Carrier (L)**  
NS Package Number E20A

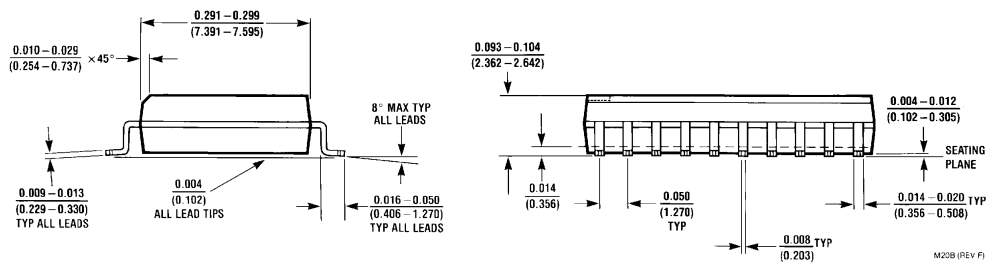
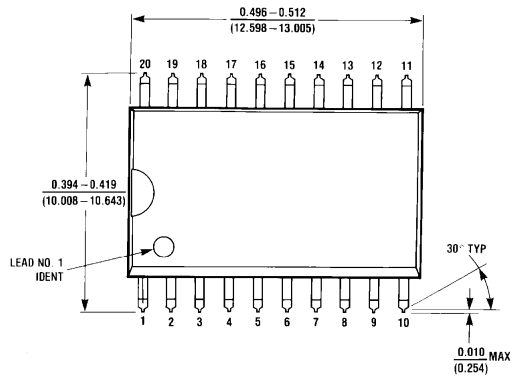
E20A (REV D)



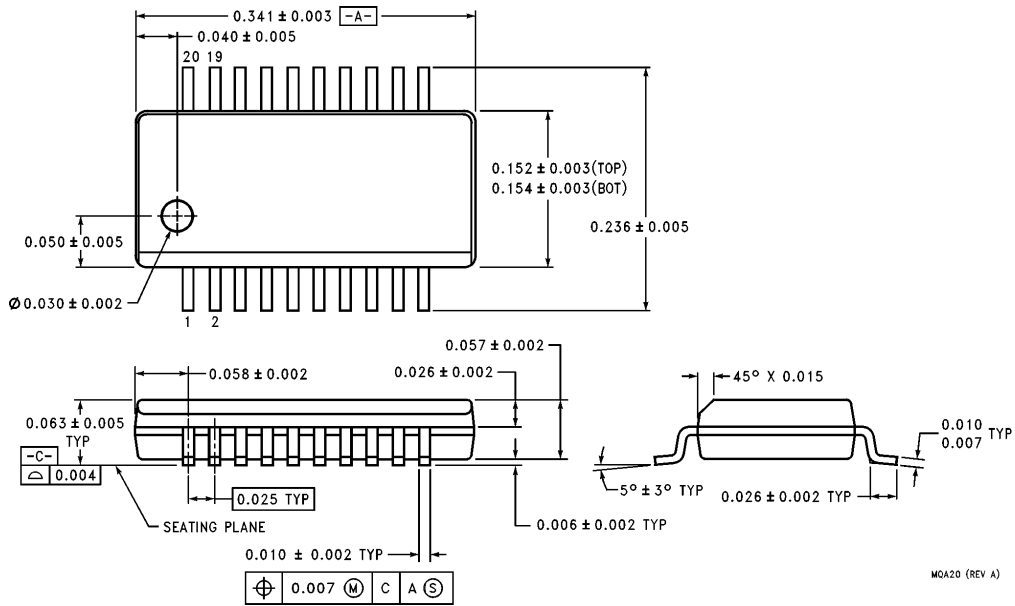
**20-Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J20A

J20A (REV M)

**Physical Dimensions** inches (millimeters) (Continued)



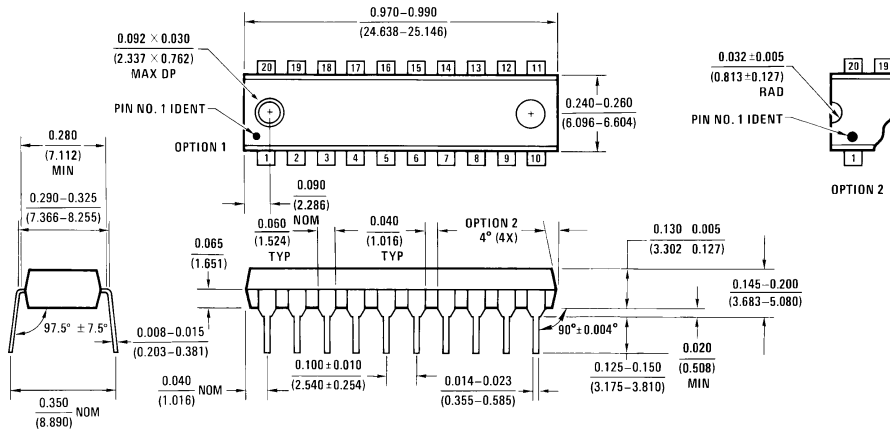
**20-Lead Small Outline Integrated Circuit (S)  
NS Package Number M20B**



**20-Lead Quarter Size Outline Package (QS)  
NS Package Number MQA20**

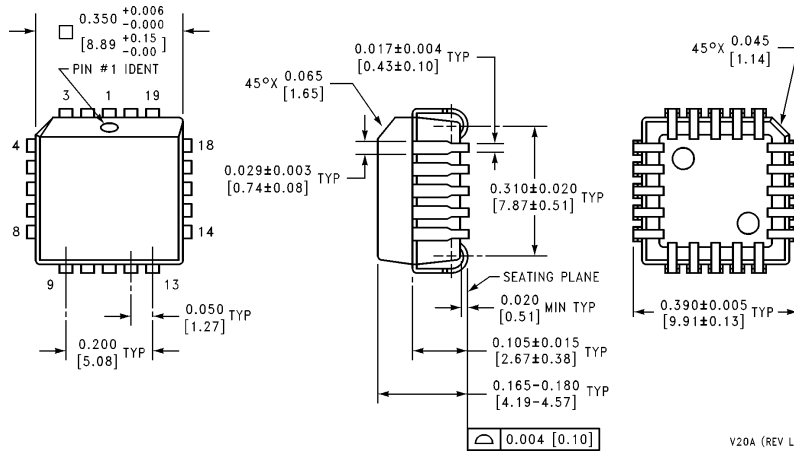


**Physical Dimensions** inches (millimeters) (Continued)



**20-Lead Plastic Dual-In-Line Package (P)**  
NS Package Number N20B

N20B (REV A)

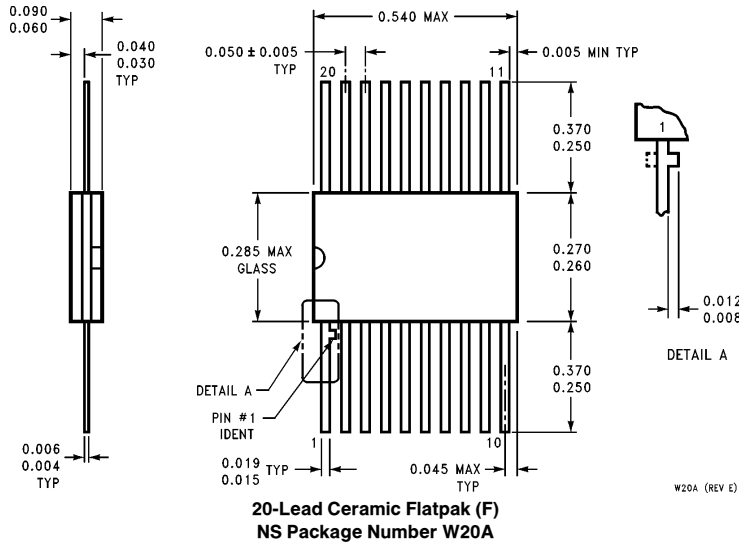


**20-Lead Plastic Chip Carrier (Q)**  
NS Package Number V20A

V20A (REV L)

**Physical Dimensions** inches (millimeters) (Continued)

Lit. # 114674



**LIFE SUPPORT POLICY**

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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Datasheets for electronics components.

# National Semiconductor was acquired by Texas Instruments.

[http://www.ti.com/corp/docs/investor\\_relations/pr\\_09\\_23\\_2011\\_national\\_semiconductor.html](http://www.ti.com/corp/docs/investor_relations/pr_09_23_2011_national_semiconductor.html)

This file is the datasheet for the following electronic components:

54ACTQ244 - <http://www.ti.com/product/54actq244?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

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