PRELIMINARY DATA

COUNTER/DIVIDERS: 4017B - DECADE COUNTER WITH 10 DECODED OUTPUTS
4022B - OCTAL COUNTER WITH 8 DECODED OUTPUTS

- FULLY STATIC OPERATION
- MEDIUM SPEED OPERATION-12 MHz (TYP.) AT V_{DD}= 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4017B/4022B** (extended temperature range) and **HCF 4017B/4022B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4017B** and **HCC/HCF 4022B** are 5-stage and 4-stage Johnson counters having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times. These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson decade-counter configuration permits high-speed operation, 2-input decimal-decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the **HCC/HCF 4017B** or every 8 clock input cycles in the **HCC/HCF 4022B** and is used to ripple-clock the succeeding device in a multi-device counting chain.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

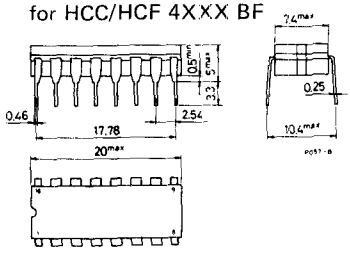
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

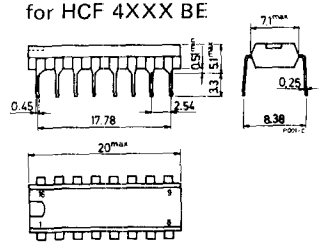
HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

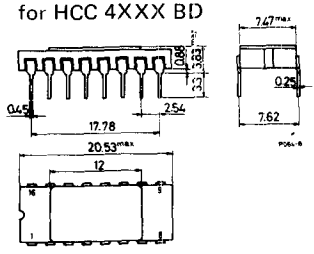
Dual in-line ceramic package
for HCC/HCF 4XXX BF



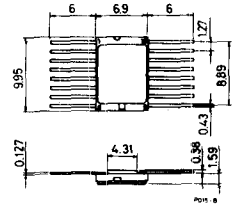
Dual in-line plastic package
for HCF 4XXX BE



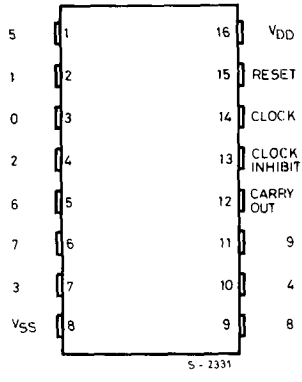
Dual in-line ceramic package
for HCC 4XXX BD



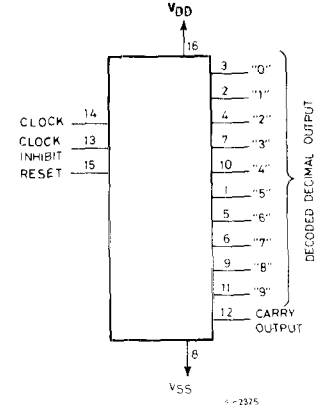
Ceramic flat package
for HCC 4XXX BK



CONNECTION DIAGRAM
for **4017B**

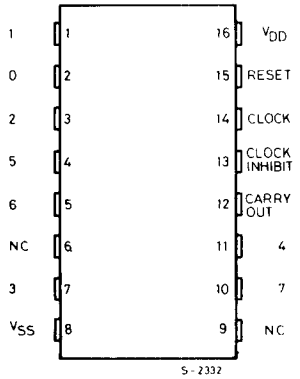


FUNCTIONAL DIAGRAM
for **4017B**



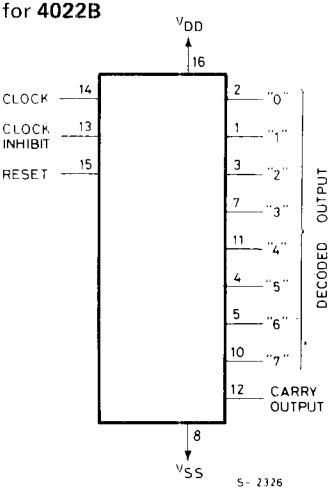
CONNECTION DIAGRAM

for **4022B**



FUNCTIONAL DIAGRAM

for **4022B**

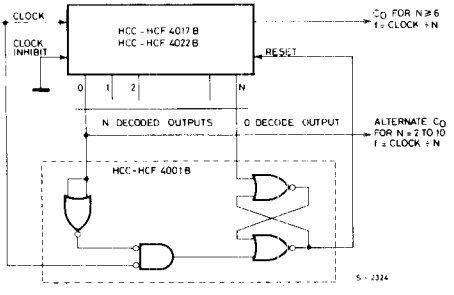


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

TYPICAL APPLICATIONS

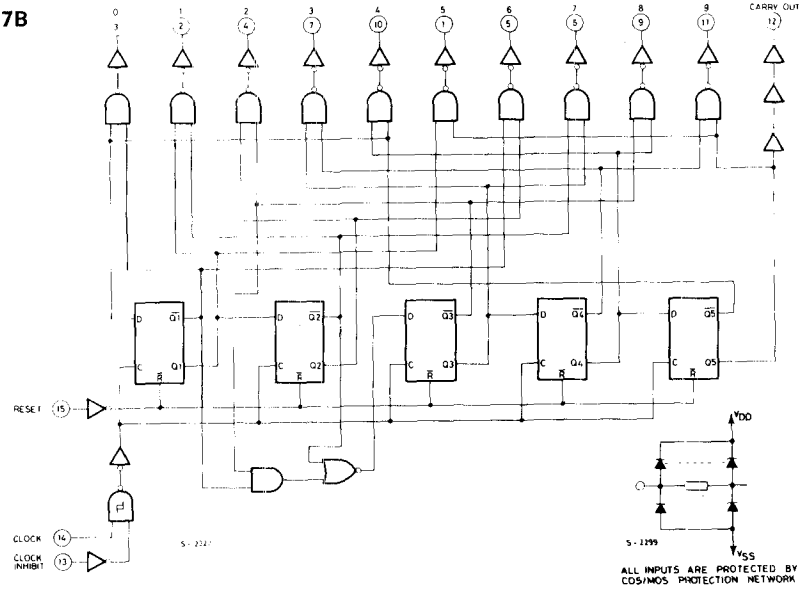
Divide by N counter ($N \leqslant 10$) with N decoded outputs



When the Nth decoded output is reached (Nth clock pulse) the S-R flip-flop (constructed from two NOR gates of the **HCC/HCF 4001B**) generates a reset pulse which clears the **HCC/HCF 4017B** to its zero count. At this time, if the Nth decoded output is greater than or equal to 6, the C_{OUT} line goes high to clock the next **HCC/HCF 4017B** counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output high resets the S-R flip flop to enable the **HCC/HCF 4017B**. If the Nth decoded output is less than 6, the C_{OUT} line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

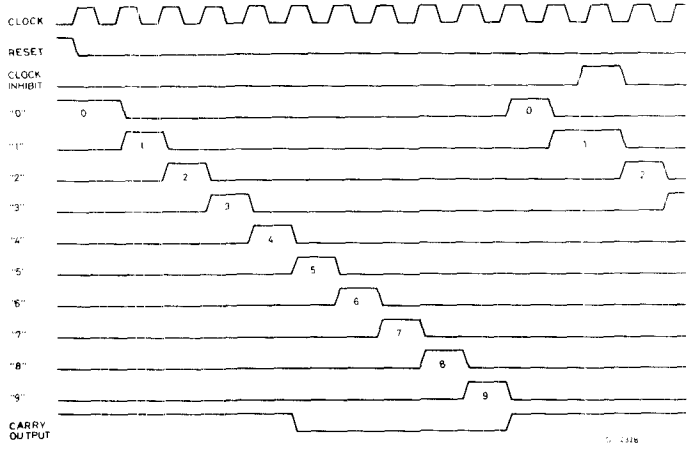
LOGIC DIAGRAM

for **4017B**



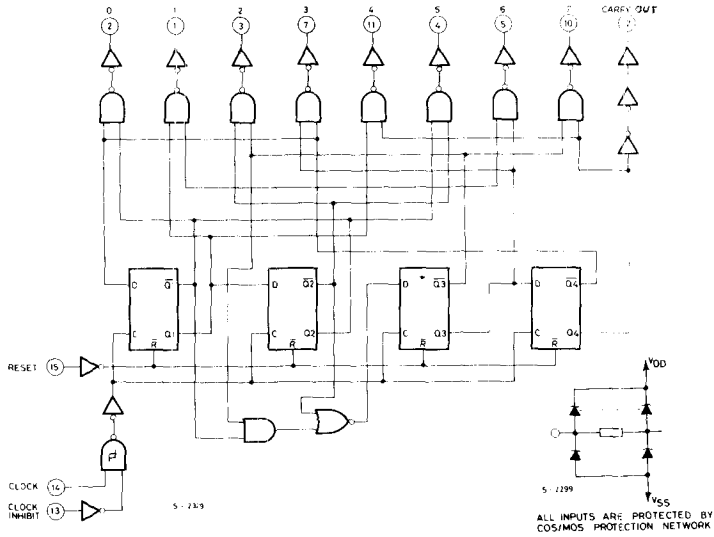
TIMING DIAGRAM

for **4017B**



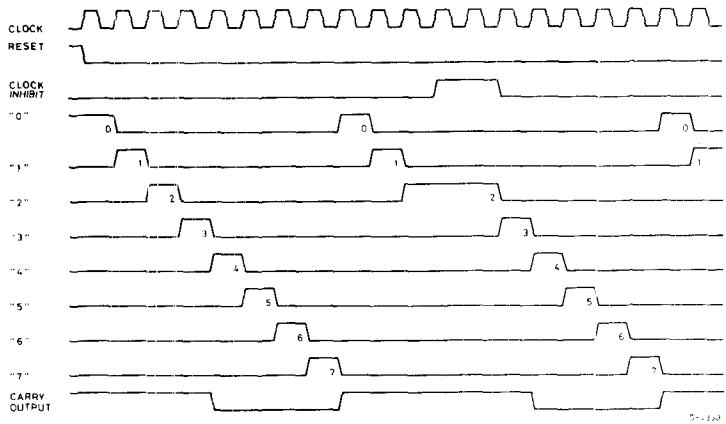
LOGIC DIAGRAM

for **4022B**



TIMING DIAGRAM

for **4022B**



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

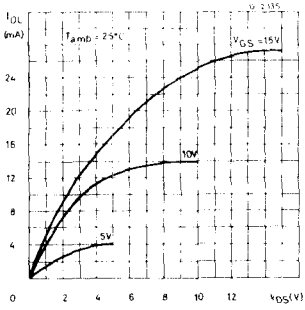
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD}= 0.3%/°C values, all input rise and fall time = 20 ns)

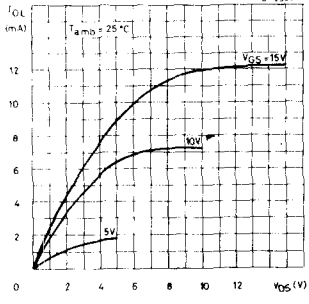
Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
CLOCKED OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time (Carry Out or Decoded cut Lines)	5		250		ns
		10		100		
		15		80		
t_{THL}, t_{TLH}	Transition time (Carry Out or Decoded Out Lines)	5		100		ns
		10		50		
		15		40		
f_{CL}*	Maximum clock input frequency	5		5		MHz
		10		12		
		15		16		
t_W	Minimum clock pulse width	5		100		ns
		10		45		
		15		30		
t_r, t_f	Clock input rise or fall time	5	Unlimited			μs
		10				
		15				
t_{setup}	Data setup time Minimum clock inhibit	5		175		ns
		10		75		
		15		50		
RESET OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time (Carry Out or Decode Out Lines)	5		250		ns
		10		100		
		15		80		
t_W	Minimum reset pulse width	5		200		ns
		10		100		
		15		75		
t_R	Minimum reset removal time	5		100		ns
		10		50		
		15		40		

* Measured with respect to carry output line.

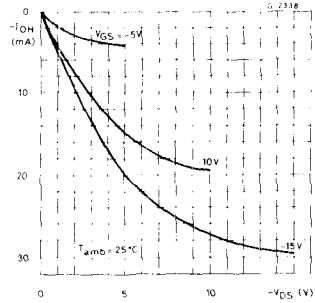
Typical output low (sink) current characteristics



Minimum output low (sink) current characteristics



Typical output high (source) current characteristics



Minimum output high (source) current characteristics