

High Speed Quad SPST CMOS Analog Switch

December 1993

Features

- Fast Switching Times, $t_{ON} = 30ns$, $t_{OFF} = 40ns$
- Low "ON" Resistance of 30Ω
- Pin Compatible with Standard HI-201
- Wide Analog Voltage Range ($\pm 15V$ Supplies) of $\pm 15V$
- Low Charge Injection ($\pm 15V$ Supplies) $10pC$
- TTL Compatible
- Symmetrical Switching Analog Current Range of $80mA$

Applications

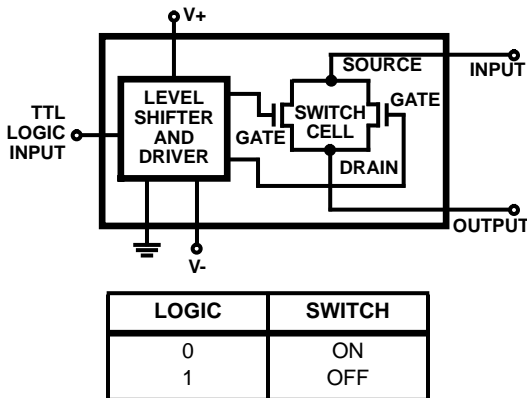
- High Speed Multiplexing
- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks
- Integrator Reset Circuits

Description

The HI-201HS is a monolithic CMOS Analog Switch featuring very fast switching speeds and low ON resistance. The integrated circuit consists of four independently selectable SPST switches and is pin compatible with the industry standard HI-201 switch.

Fabricated using silicon-gate technology and the Harris Dielectric Isolation process, this TTL compatible device offers improved performance over previously available CMOS analog switches. Featuring maximum switching times of $50ns$, low ON resistance of 50Ω maximum, and a wide analog signal range, the HI-201HS is designed for any application where improved switching performance, particularly switching speed, is required. (A more detailed discussion on the design and application of the HI-201HS can be found in Application Note 543.)

Functional Diagram

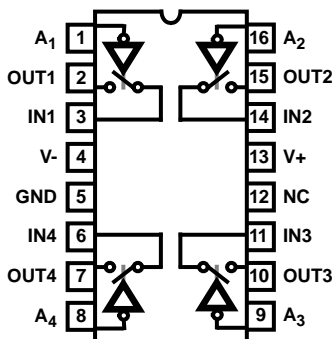


Ordering Information

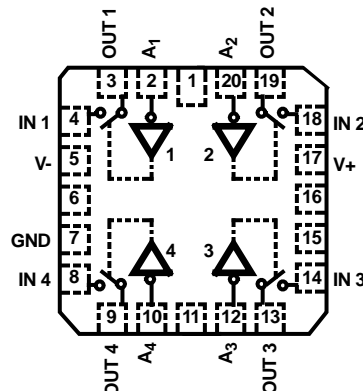
PART NUMBER	TEMP. RANGE	PACKAGE
HI1-0201HS-5	0°C to +75°C	16 Lead Ceramic DIP
HI3-0201HS-4	-25°C to +85°C	16 Lead Plastic DIP
HI1-0201HS-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0201HS-4	-25°C to +85°C	16 Lead Ceramic DIP
HI4P0201HS-5	0°C to +75°C	20 Lead PLCC
HI3-0201HS-5	0°C to +75°C	16 Lead Plastic DIP
HI1-0201HS-7	0°C to +75°C	16 Lead Ceramic DIP
HI4-0201HS/883	-55°C to +125°C	20 Lead LCC
HI9P0201HS-5	0°C to +75°C	16 Lead SOIC (W)
HI9P0201HS-9	-40°C to +85°C	16 Lead SOIC (W)
HI1-0201HS/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0201HS -8	-55°C to +125°C	16 Lead Ceramic DIP

Pinouts

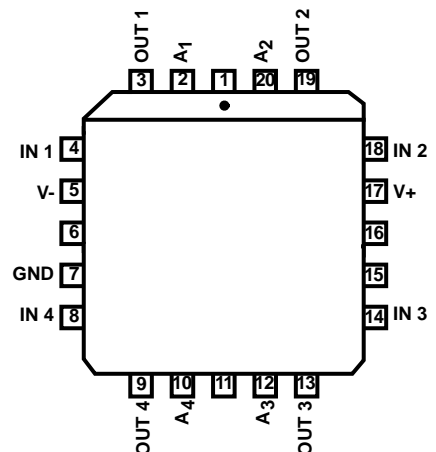
HI-201HS (CDIP, PDIP, SOIC)
TOP VIEW



HI201HS (LCC)
TOP VIEW

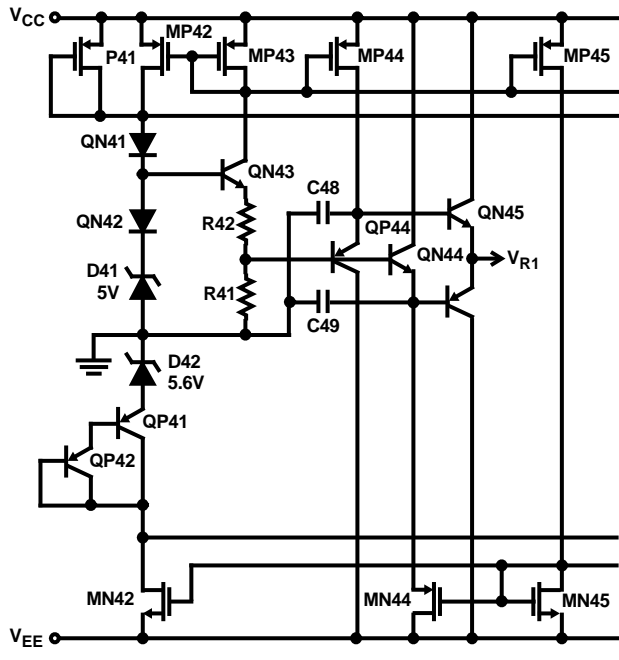


HI201HS (PLCC)
TOP VIEW

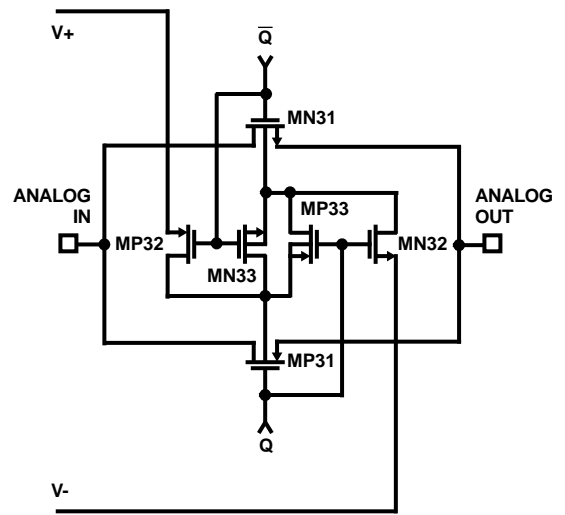


Schematic Diagrams

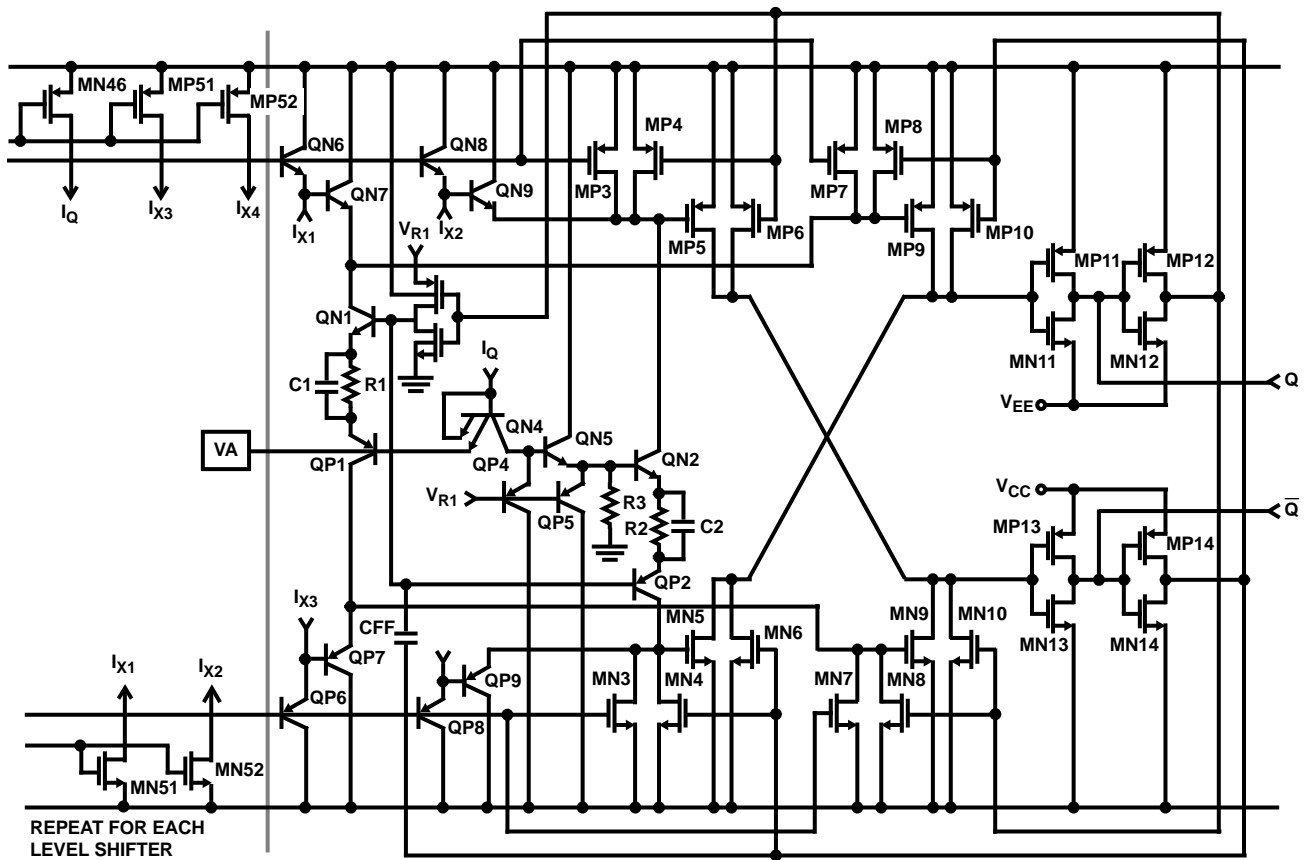
TTL/CMOS REFERENCE CIRCUIT



SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Specifications HI-201HS

Absolute Maximum Ratings

Supply Voltage (Between Pins 4 and 13)	36V
Digital Input Voltage (Pins 1, 8, 9, 16)	(V+) +4V, (V-) -4V
Analog Input Voltage (One Switch)	(V+) +2.0V
Pins 2, 3, 6, 7, 10, 11, 14, 15	(V-) -2.0V
Peak Current (S or D)	
(Pulse at 1ms, 10% Duty Cycle Max.)	50mA
Continuous Current Any Terminal (Except S or D)	25mA
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering 10s)	+300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP	80°C/W	24°C/W
Plastic DIP	100°C/W	-
PLCC	80°C/W	-
SOIC	100°C/W	-
Operating Temperature		
HI-201HS-2,-8	-55°C to +125°C	
HI-201HS-4	-25°C to +85°C	
HI-201HS-5,-7	0°C to +75°C	
HI-201HS-9	-40°C to +85°C	
Junction Temperature		
Ceramic Package	+175°C	
Plastic Package	+150°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, GND = 0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP	HI-201HS-2/-8			HI-201HS-5/-4/-9/-7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
t_{ON} , Switch On Time	(Note 3)	+25°C	-	30	50	-	30	50	ns
t_{OFF1} , Switch Off Time	(Note 3)	+25°C	-	40	50	-	40	50	ns
t_{OFF2} , Switch Off Time	(Note 3)	+25°C	-	150	-	-	150	-	ns
Output Settling Time 0.1%		+25°C	-	180	-	-	180	-	ns
"Off Isolation"	(Note 4)	+25°C	-	72	-	-	72	-	dB
Crosstalk	(Note 5)	+25°C	-	86	-	-	86	-	dB
Charge Injection	(Note 6)	+25°C	-	10	-	-	10	-	pC
$C_{S(OFF)}$, Input Switch Capacitance		+25°C	-	10	-	-	10	-	pF
$C_{D(OFF)}$, } Output Switch Capacitance		+25°C	-	10	-	-	10	-	pF
	$C_{D(ON)}$, }	+25°C	-	30	-	-	30	-	pF
C_A , Digital Input Capacitance		+25°C	-	18	-	-	18	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance		+25°C	-	0.5	-	-	0.5	-	pF
DIGITAL INPUT CHARACTERISTICS									
V_{AL} , Input Low Threshold		Full	-	-	0.8	-	-	0.8	V
V_{AH} , Input High Threshold		+25°C	2.0	-	-	2.0	-	-	V
		Full	2.4	-	-	2.4	-	-	V
I_{AL} , Input Leakage Current (Low)		+25°C	-	-200	-	-	-200	-	μA
		Full	-	-	-500	-	-	-500	μA
I_{AH} , Input Leakage Current (High)	$V_{AH} = 4.0V$	+25°C	-	20	-	-	20	-	μA
		Full	-	-	+40	-	-	+40	μA
ANALOG SWITCH CHARACTERISTICS									
V_S , Analog Signal Range		Full	-15	-	+15	-15	-	+15	V
R_{ON} , On Resistance	(Note 2)	+25°C	-	30	50	-	30	50	Ω
		Full	-	-	75	-	-	75	Ω
R_{ON} Match		+25°C	-	3	-	-	3	-	%

Specifications HI-201HS

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, GND = 0V, Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP	HI-201HS-2/-8			HI-201HS-5/-4/-9/-7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{S(OFF)}$, Off Input Leakage Current		+25°C	-	0.3	10	-	0.3	10	nA
		Full	-	-	100	-	-	50	nA
$I_{D(OFF)}$, Off Output Leakage Current		+25°C	-	0.3	10	-	0.3	10	nA
		Full	-	-	100	-	-	50	nA
$I_{D(ON)}$, On Leakage Current		+25°C	-	0.1	10	-	0.1	10	nA
		Full	-	-	100	-	-	50	nA
POWER SUPPLY CHARACTERISTICS (Note 7)									
P_D , Power Dissipation		+25°C	-	120	-	-	120	-	mW
		Full	-	-	240	-	-	240	mW
I_+ , Current (Pin 13)		+25°C	-	4.5	-	-	4.5	-	mA
		Full	-	-	10.0	-	-	10.0	mA
I_- , Current (Pin 4)		+25°C	-	3.5	-	-	3.5	-	mA
		Full	-	-	6	-	-	6	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $V_{OUT} = \pm 10V$, $I_{OUT} = 1mA$.
3. $R_L = 1k\Omega$, $C_L = 35pF$, $V_{IN} = +10V$, $V_A = +3V$. (See Switching Waveforms).
4. $V_A = 3V$, $R_L = 1k\Omega$, $C_L = 10pF$, $V_{IN} = 3V_{RMS}$, $f = 100kHz$.
5. $V_A = 3V$, $R_L = 1k\Omega$, $V_{IN} = 3V_{RMS}$, $f = 100kHz$.
6. $C_L = 1000pF$, $V_{IN} = 0V$, $R_{IN} = 0V$, $\Delta Q = C_L \times \Delta V_O$.
7. $V_A = 3V$ or $V_A = 0$ for all switches.

Switching Waveforms

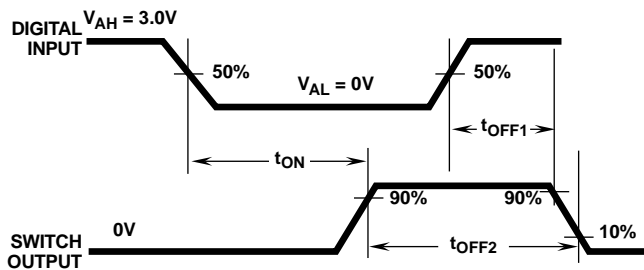
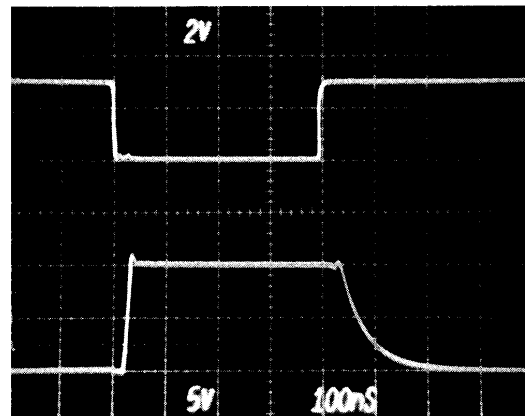


FIGURE 1A.



TOP: TTL Input (2V/Div.) BOTTOM: Output (5V/Div.)
HORIZONTAL: 100ns/Div.

FIGURE 1B.

FIGURE 1. SWITCH t_{ON} AND t_{OFF} TIMES

Typical Performance Curves

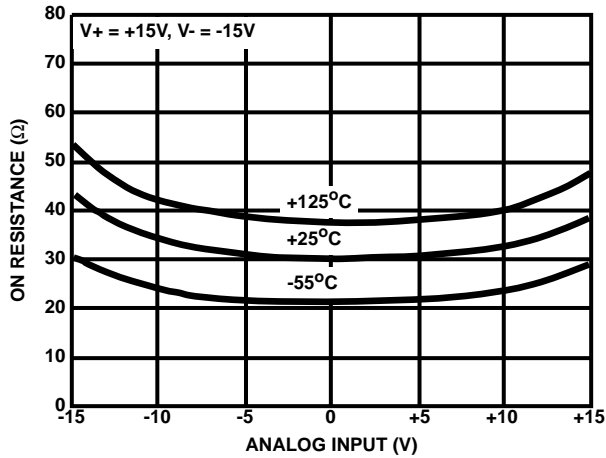


FIGURE 2. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL AND TEMPERATURE

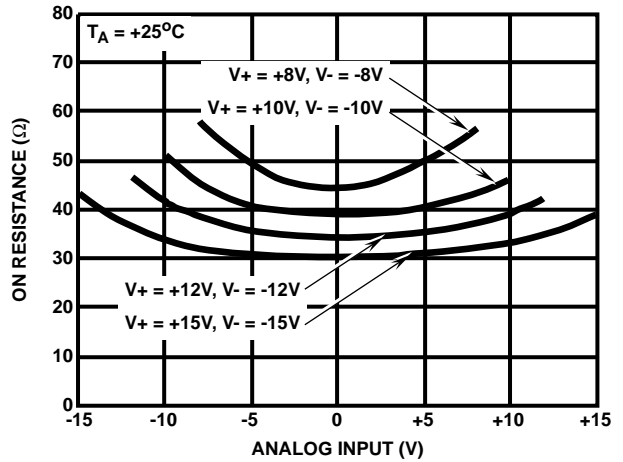


FIGURE 3. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

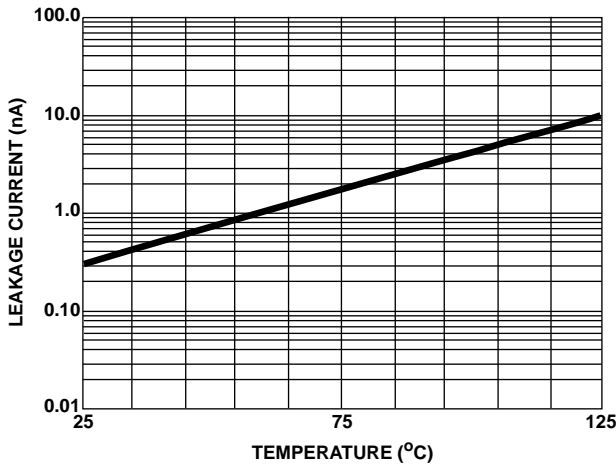


FIGURE 4. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE†

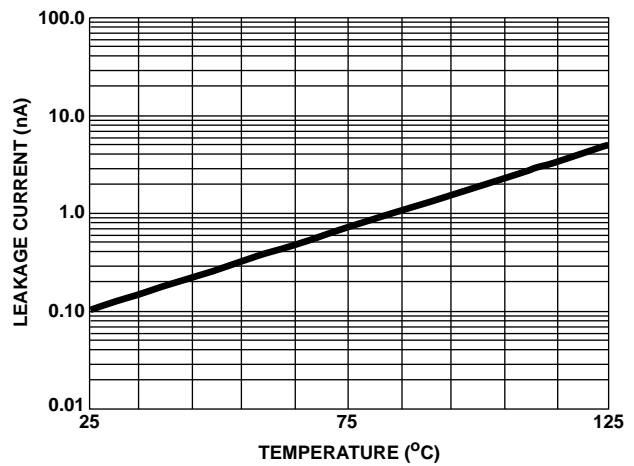


FIGURE 5. $I_{D(ON)}$ vs TEMPERATURE†

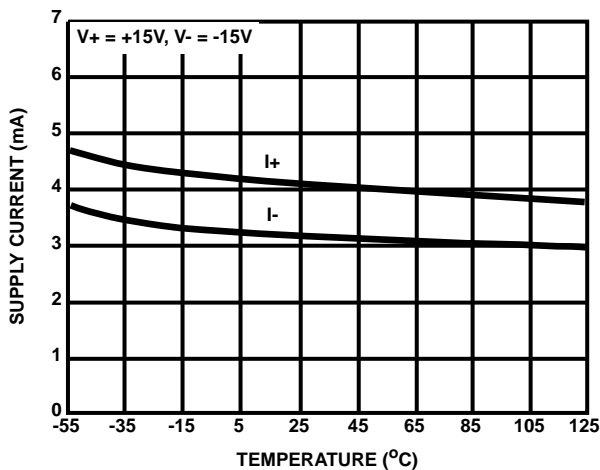


FIGURE 6. SUPPLY CURRENT vs TEMPERATURE

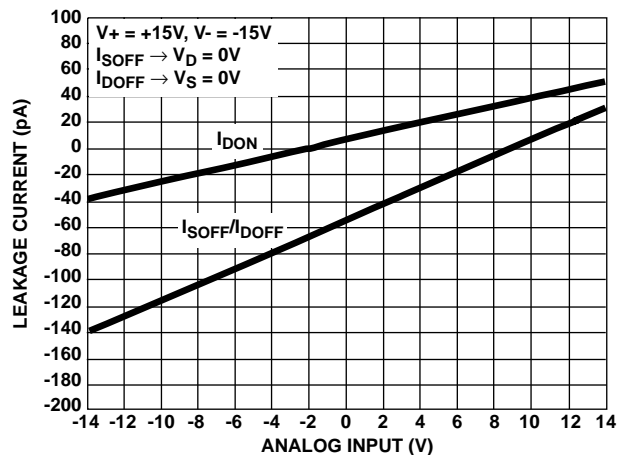


FIGURE 7. LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE

† Theoretically, leakage current will continue to decrease below +25°C. But due to environmental conditions, leakage measurements below this temperature are not representative of actual switch performance.

Typical Performance Curves (Continued)

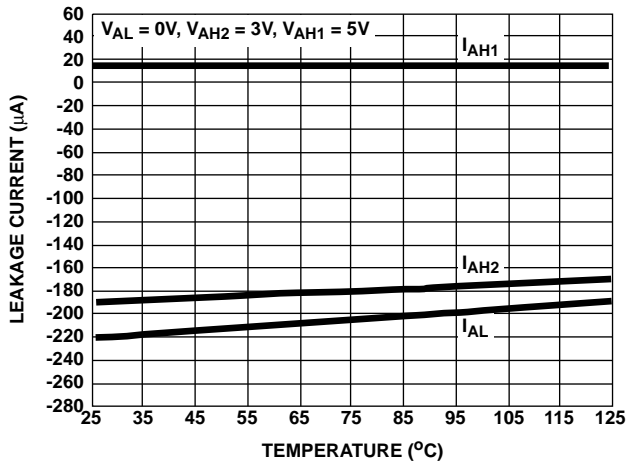


FIGURE 8. DIGITAL INPUT LEAKAGE CURRENT vs TEMPERATURE†

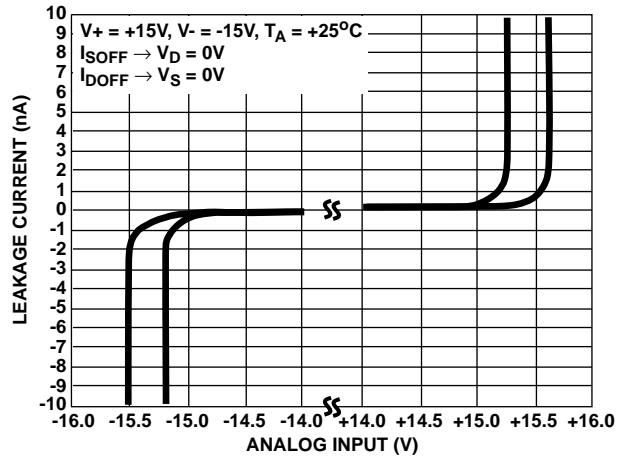


FIGURE 9. LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE

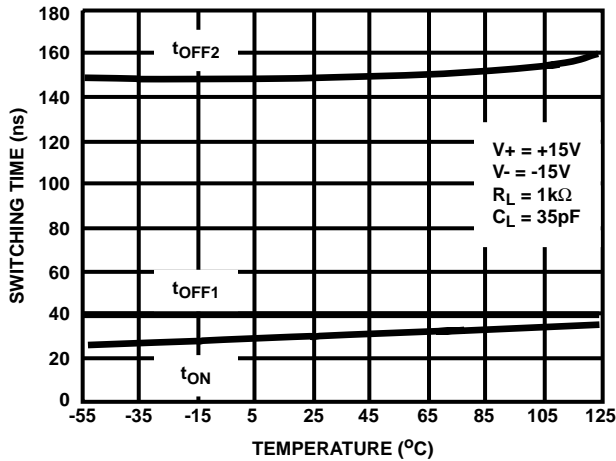


FIGURE 10. SWITCHING TIME vs TEMPERATURE

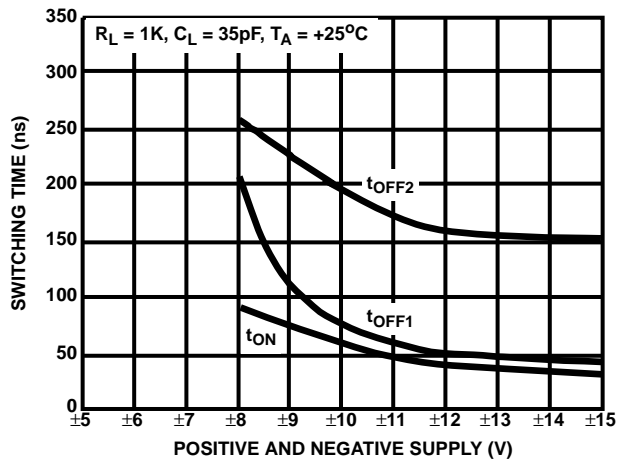


FIGURE 11. SWITCHING TIME vs POSITIVE AND NEGATIVE SUPPLY VOLTAGE

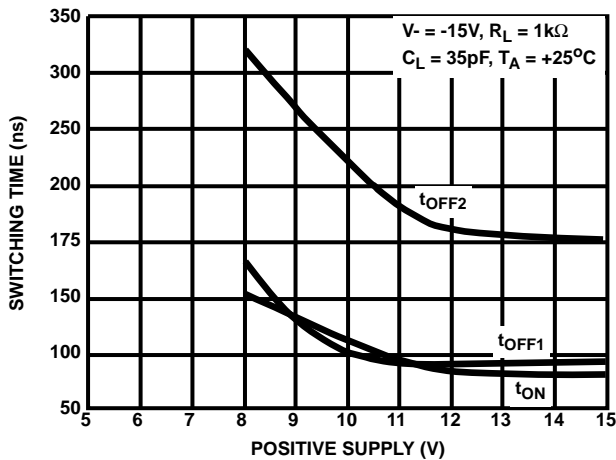


FIGURE 12. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE

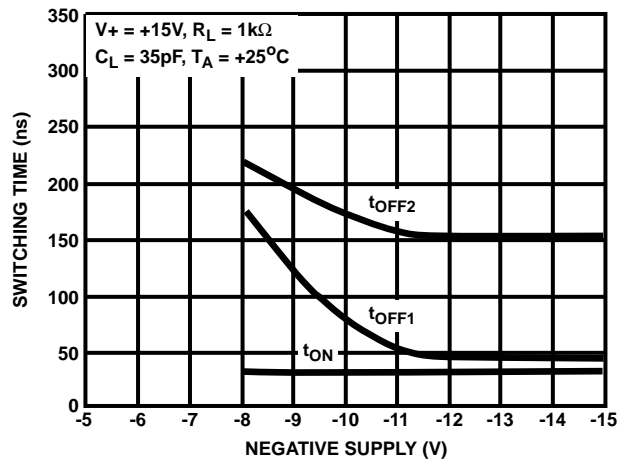


FIGURE 13. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

† Theoretically, leakage current will continue to decrease below +25°C. But due to environmental conditions, leakage measurements below this temperature are not representative of actual switch performance.

Typical Performance Curves (Continued)

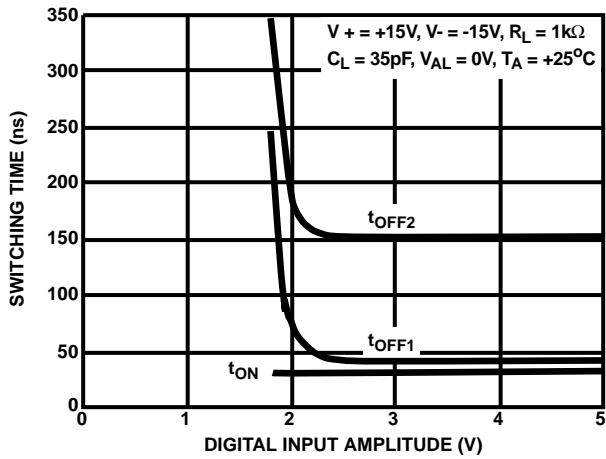


FIGURE 14. SWITCHING TIME vs INPUT LOGIC AMPLITUDE

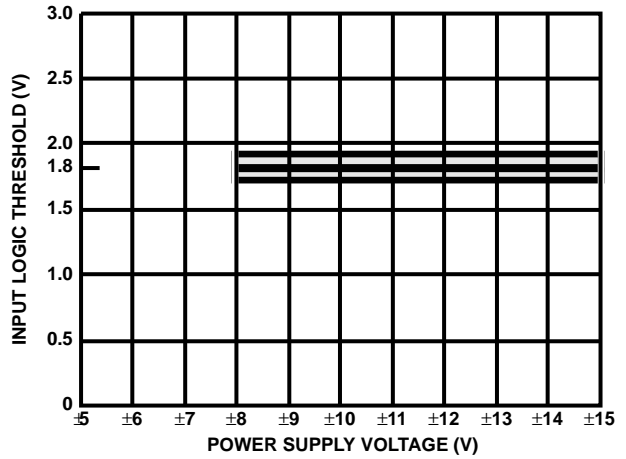


FIGURE 15. INPUT SWITCHING THRESHOLD vs POSITIVE AND NEGATIVE SUPPLY VOLTAGES

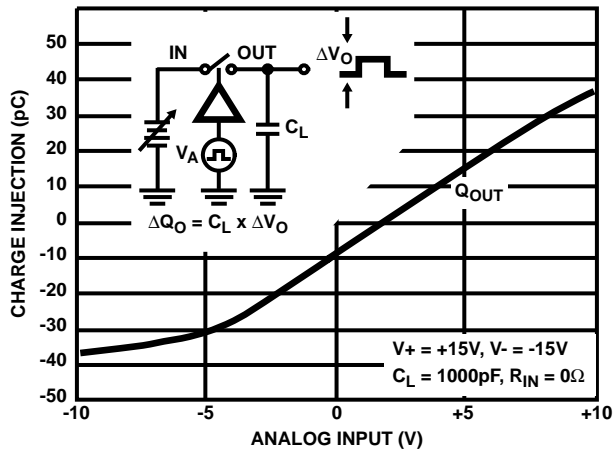


FIGURE 16. CHARGE INJECTION vs ANALOG INPUT

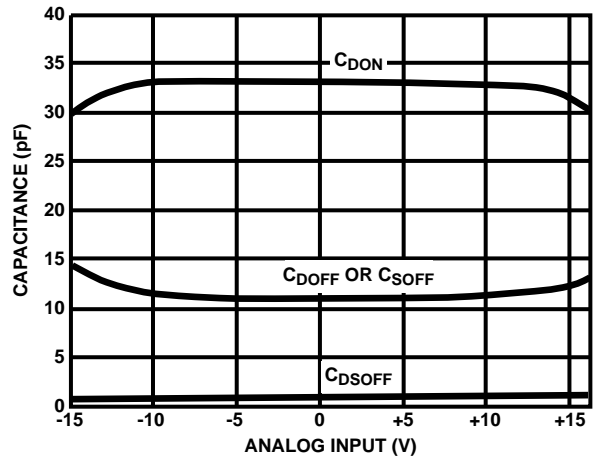


FIGURE 17. CAPACITANCE vs ANALOG INPUT

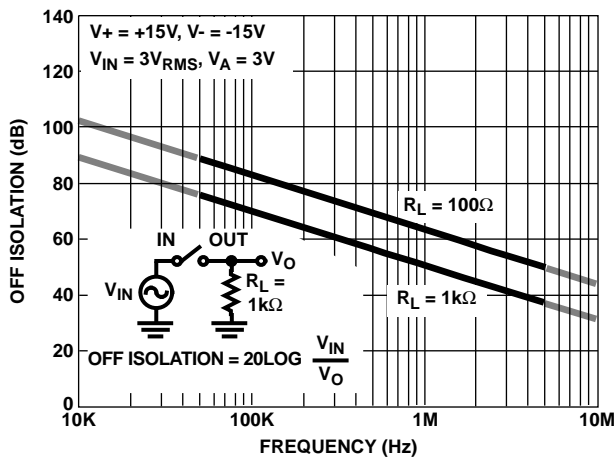


FIGURE 18. OFF ISOLATION vs FREQUENCY

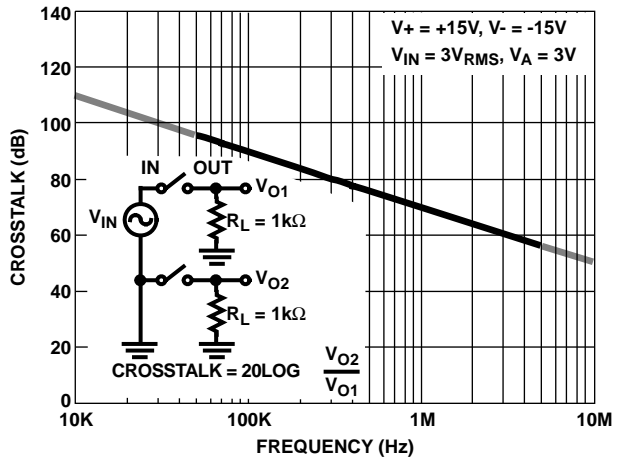


FIGURE 19. CROSSTALK vs FREQUENCY

Test Circuit

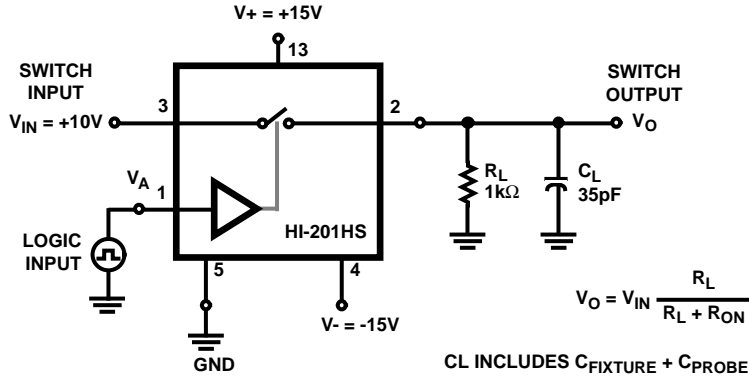


FIGURE 20. SWITCHING TEST CIRCUIT (t_{ON} , t_{OFF1} , t_{OFF2})

Switching Characteristics

Typical delay, t_{ON} , t_{OFF} , settling time and switching transients in this circuit. If R_L or C_L is increased, there will be corresponding increases in rise and/or fall RC times..

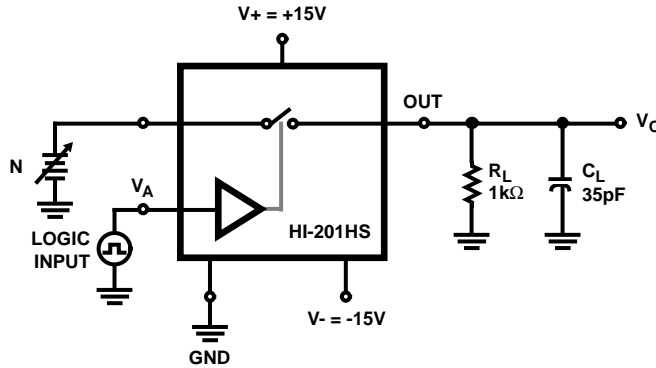


FIGURE 21A.

LOGIC INPUT

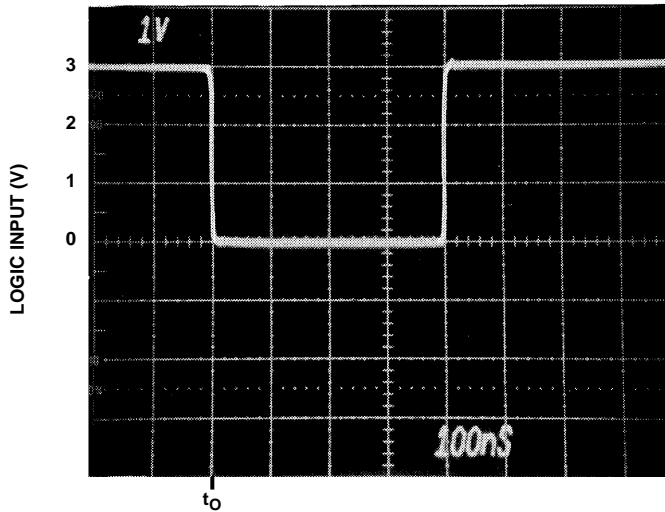
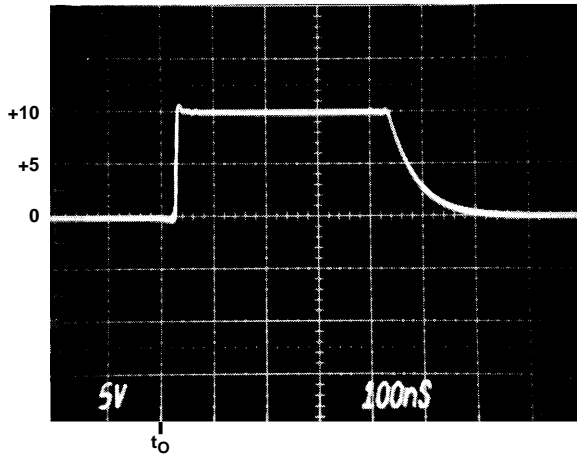


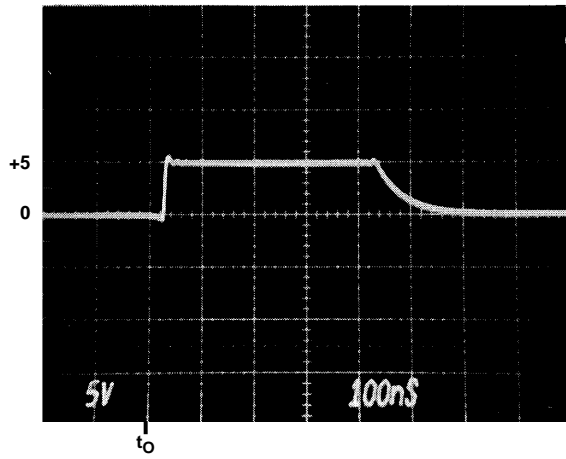
FIGURE 21B.

FIGURE 21. SWITCHING CHARACTERISTICS vs INPUT VOLTAGE

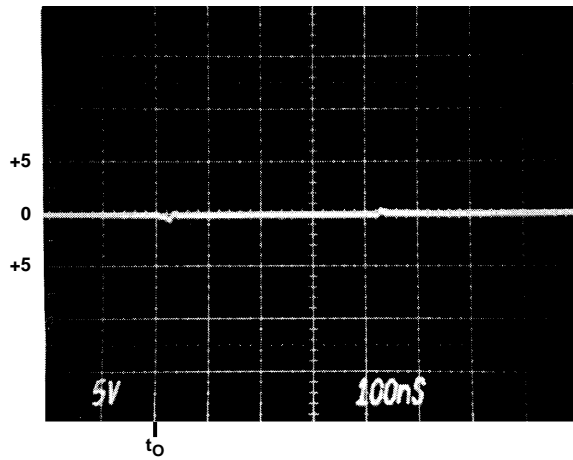
Switching Characteristics (Continued)



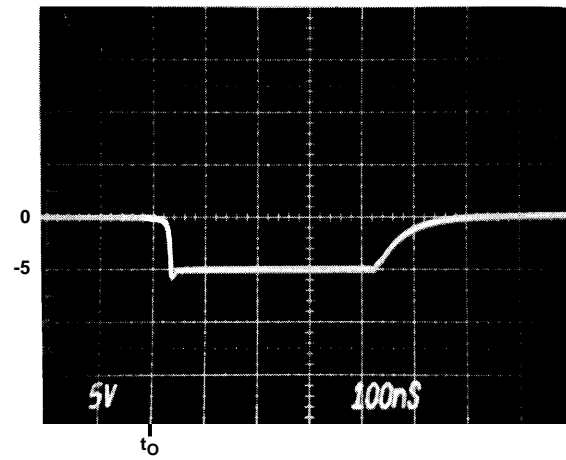
22A. $V_{IN} = +10V$



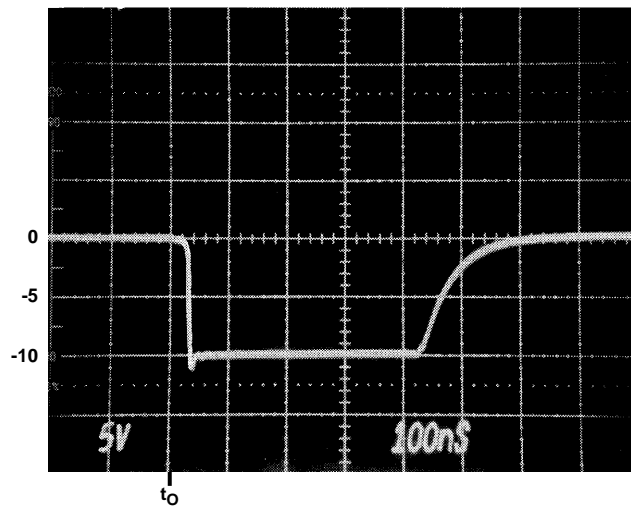
22B. $V_{IN} = +5V$



22C. $V_{IN} = 0V$



22D. $V_{IN} = -5V$



22E. $V_{IN} = -10V$

FIGURE 22. V_O - OUTPUT SWITCHING WAVEFORMS

HI-201HS

Application Information

Logic Compatibility

The HI-201HS is TTL compatible. Its logic inputs (Pins 1, 8, 9, 16) are designed to react to digital inputs which exceed a fixed, internally generated TTL switching threshold. The HI-201HS can also be driven with CMOS logic (0V-15V), although the switch performance with CMOS logic will be inferior to that with TTL logic (0V-5V).

The logic input design of the HI-201HS is largely responsible for its fast switching speed. It is a design which features a unique input stage consisting of complementary vertical PNP and NPN bipolar transistors. This design differs from that of the standard HI-201 product where the logic inputs are MOS transistors.

Although the new logic design enhances the switching speed performance, it also increases the logic input leakage currents. Therefore, the HI-201HS will exhibit larger digital input leakage currents in comparison to the standard HI-201 product.

Charge Injection

Charge injection is the charge transferred, through the internal gate-to-channel capacitances, from the digital logic input to the analog output. To optimize charge injection performance for the HI-201HS, it is advisable to provide a TTL logic input with fast rise and fall times.

If the power supplies are reduced from $\pm 15V$, charge injection will become increasingly dependent upon the digital input frequency. Increased logic input frequency will result in larger output error due to charge injection.

Power Supply Considerations

The electrical characteristics specified in this data sheet are guaranteed for power supplies $\pm V_S = \pm 15V$. Power supply voltages less than $\pm 15V$ will result in reduced switch performance. The following information is intended as a design aid only.

POWER SUPPLY VOLTAGES	SWITCH PERFORMANCE
$\pm 12 < \pm V_S \pm 15V$	Minimal Variation
$\pm V_S < \pm 12V$	Parametric variation becomes increasingly large (increased ON resistance, longer switching times).
$\pm V_S < \pm 10V$	Not Recommended.
$\pm V_S > \pm 16V$	Not Recommended.

Single Supply

The switch operation of the HI-201HS is dependent upon an internally generated switching threshold voltage optimized for $\pm 15V$ power supplies. The HI-201HS does not provide the necessary internal switching threshold in a single supply system. Therefore, if single supply operation is required, the HI-300 series of switches is recommended. The HI-300 series will remain operational to a minimum +5V single supply.

Switch performance will degrade as power supply voltage is reduced from optimum levels ($\pm 15V$). So it is recommended that a single supply design be thoroughly evaluated to ensure that the switch will meet the requirements of the application.

For Further Information See Application Notes 520, 521, 531, 532, 543 and 557.

HI-201HS

Die Characteristics

DIE DIMENSIONS:

2440 μ m x 2860 μ m x 485 μ m \pm 25 μ m

METALLIZATION:

Type: CuAl

Thickness: 16k \AA \pm 2k \AA

GLASSIVATION:

Type: Nitride Over Silox

Nitride Thickness: 3.5k \AA \pm 1k \AA

Silox Thickness: 12k \AA \pm 2k \AA

WORST CASE CURRENT DENSITY:

9.5 x 10⁴A/cm²

Metallization Mask Layout

HI-201HS

